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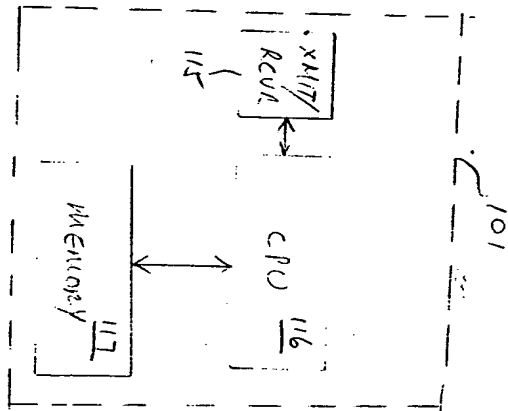
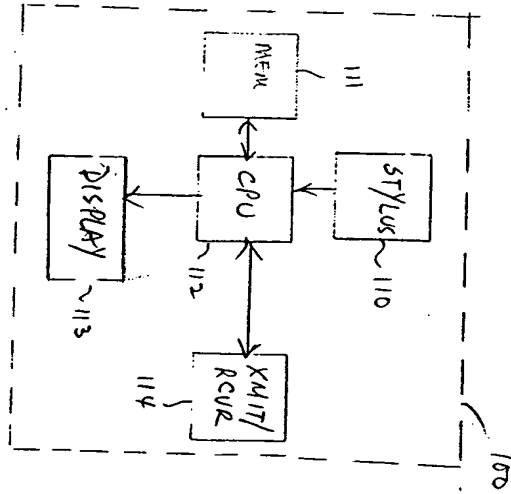


FIGURE 1a

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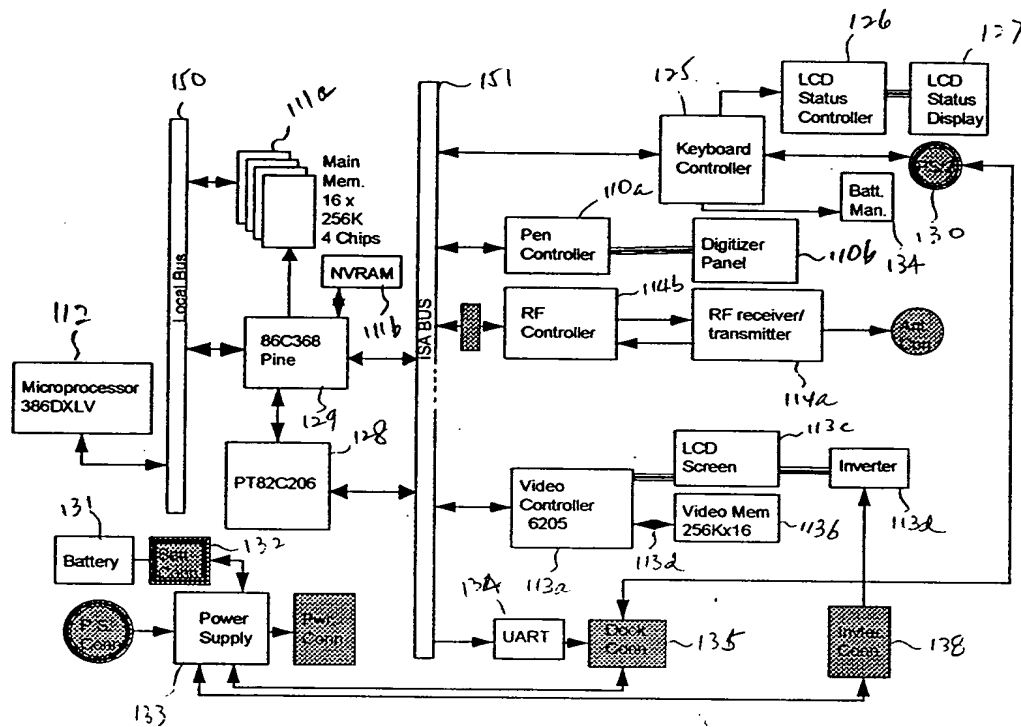


FIGURE 1b

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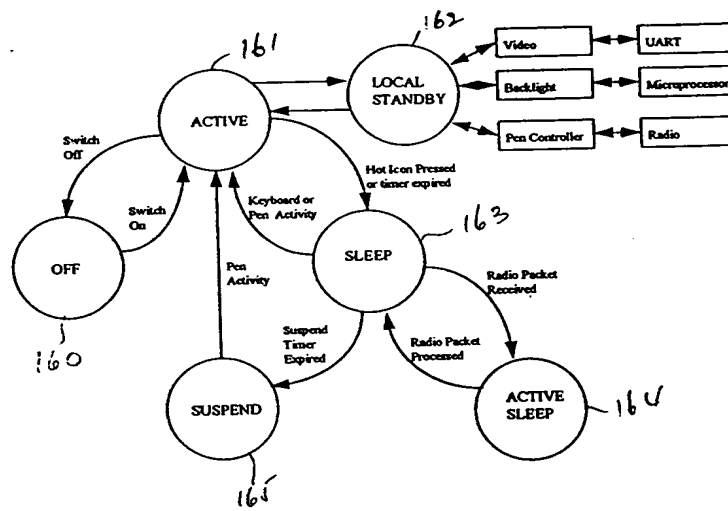


FIGURE 1c

Device	State	Clocks Disabled	Comments	Wakeup Source
Microprocessor	Static Suspend	Clock Stop Control by 368	Static Mode entered when clock stopped	Clock Restarted and Controlled by 368
PICO 368	Static Suspend	Clock Stopped/ 32KHz Left on		Activity on EXACT, SWITCH, or RING pins
82C206	Static	32khz Source		Any Interrupts
Main Memory	Slow Refresh	Pico368 38khz	Memory Refreshed at 128mS	
Video	Static	14 Mhz disconnected	Controlled through use of Evergreen 368 power management pins.	When system is resumed
Video Memory	Slow Refresh	32khz	Memory Refreshed at 128mS	Video Controller
				automatically adjusts refresh rate depending on mode
LCD Module	OFF	NA	Power to Module will never be applied in Sleep	Controlled by Video controller power up sequencing
LCD Backlight	OFF	NA	Backlight will never be on in Sleep	Controlled by Video controller power up sequencing
UART	Static	1.84Mhz	Part has no direct power management.	
UART Trans.	Off	NA	Part turned off, until access to UART. Inactivity timer will start, and look for a time-out of two minutes before turning off transceiver.	Access to serial port
ROM	Static	NA	After ROM is shadowed, the CS and OE line will be driven high to keep these parts in a static mode.	
NVRAM	Static	NA	After NVRAM is read, the CS line will be high which forces part into a static mode.	
Pen Controller	Sleep	Own 4.0mhz	Sleeps after each point is processed as long as the pen is not pressing the screen.	Pen Down wakes up Pen controller. Pen controller asserts the PEN_ACTIVITY signal which will wake up the entire system.
Hook	Active	Own 32khz	Keeps the last display as told by the keyboard controller	NA
Clock Generator	Active	All Clocks Running	Clocks needed in order to wake system back up.	
Radio	Sleep	Internal	Radio Handles its own power management	Wakes up on periodic basis in order to keep SYNC. When a packet is ready, the Radio will assert the activity pin to the RING input of the 368 which will wake up the system

FIGURE 12

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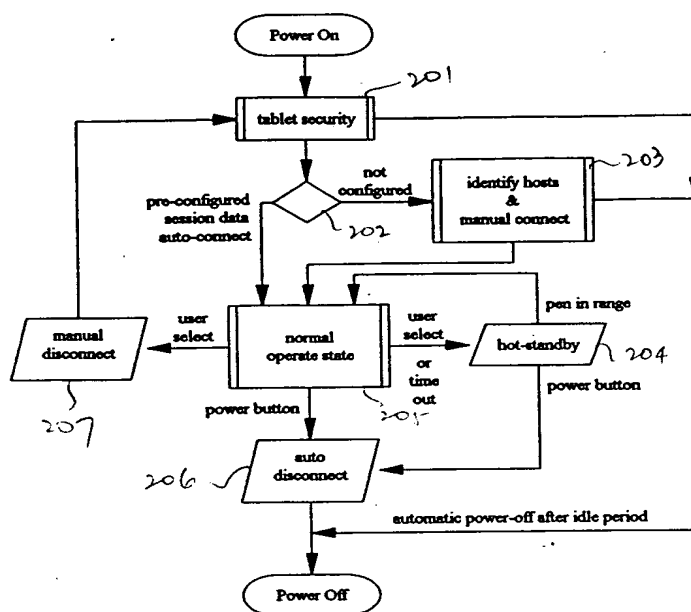


FIGURE 2

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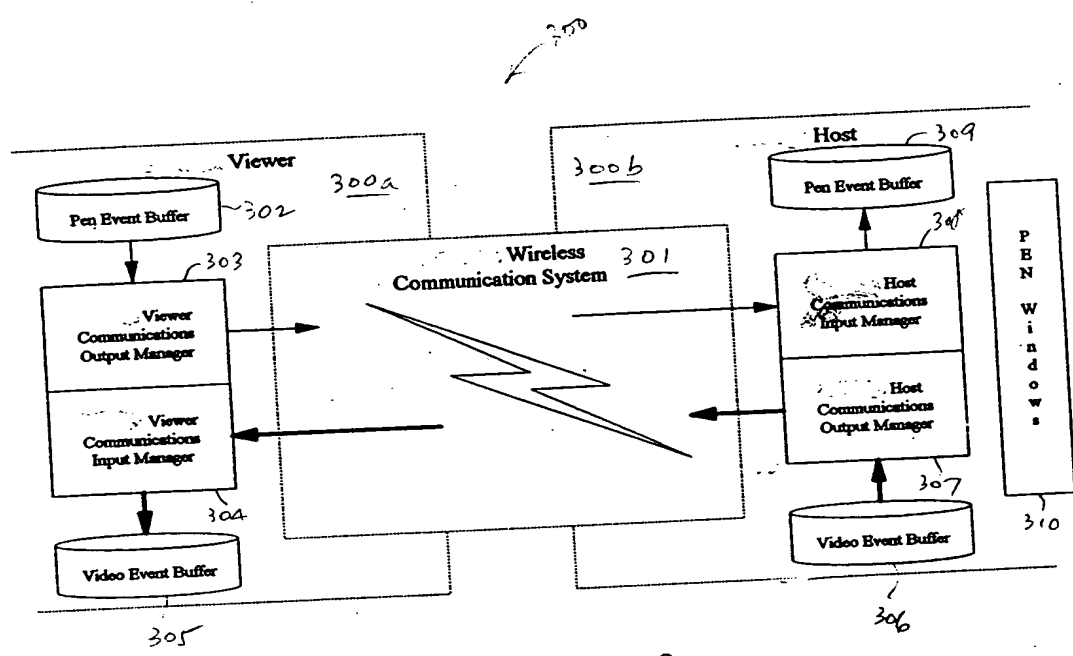


FIGURE 3a

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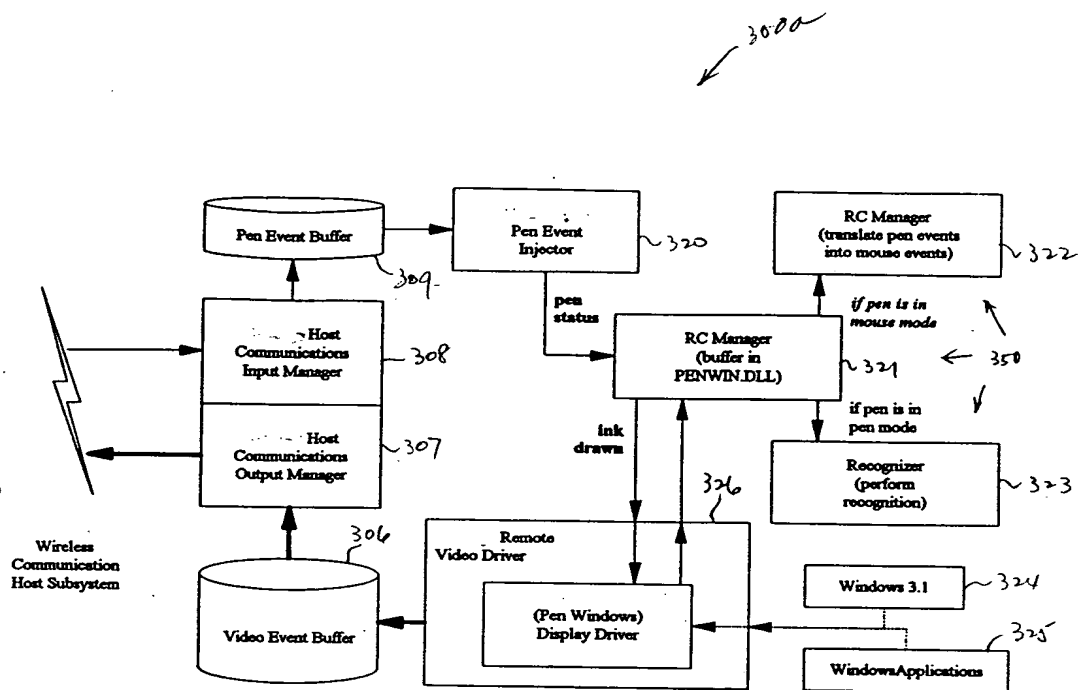


Figure 5b

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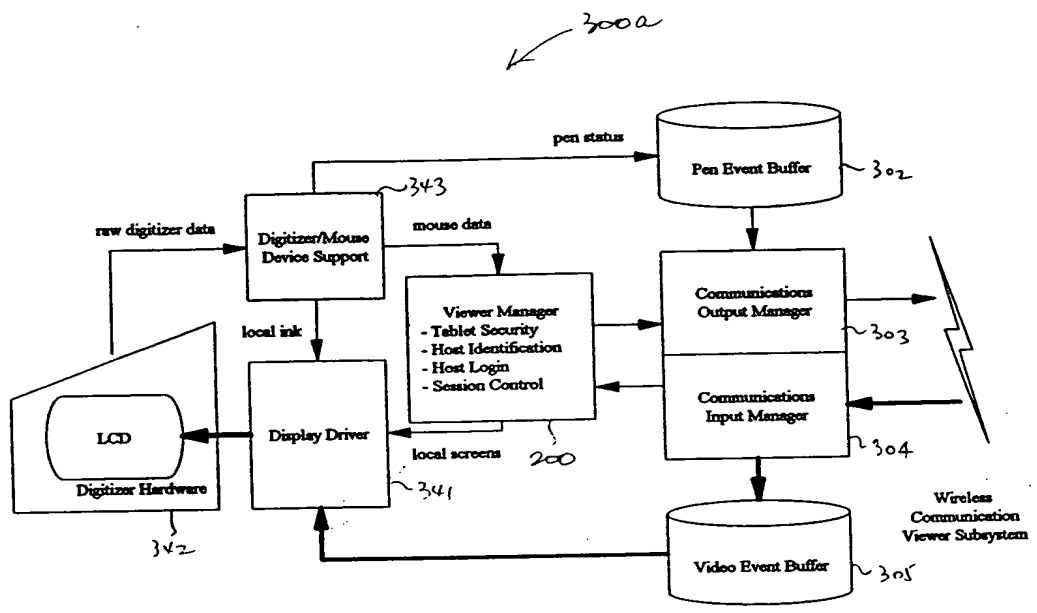


FIGURE 3c



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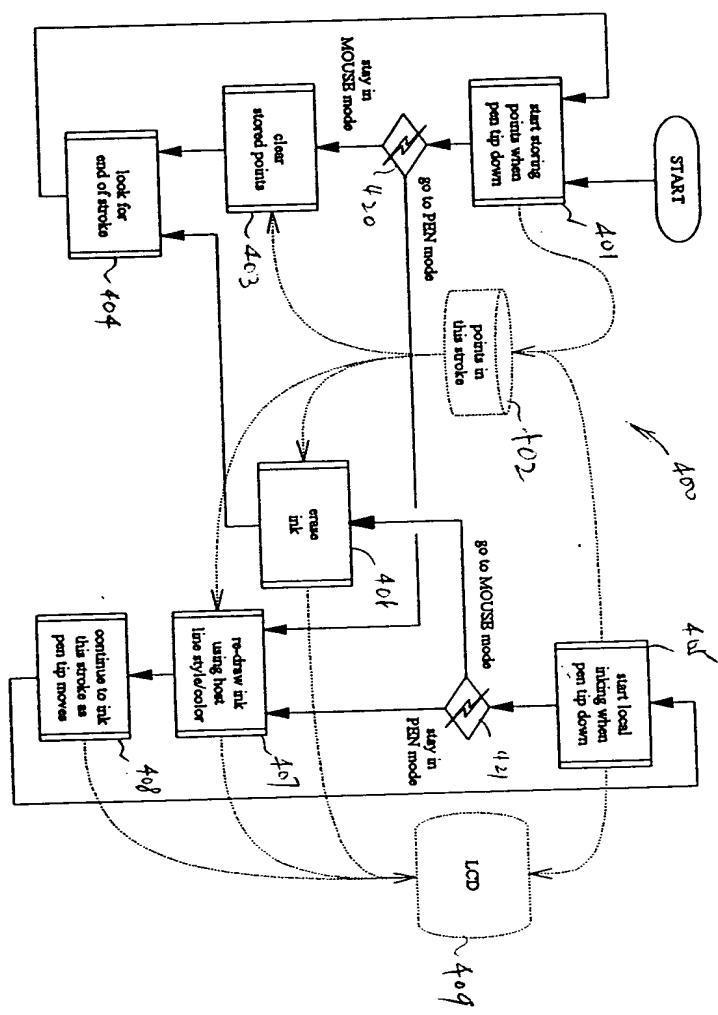


FIGURE 4